Minimization of Switching Losses of Boost Converters

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Abstract

This paper deals with the operation and analysis of a DC-DC Boost converter with the aid of Or CAD-PSpice environment in order to improve its operation. The goal is to minimize the switching losses, the weight and volume given by the passive elements, such as: filters and heat sinks. The sizing of these elements and the switching losses are proportional to the switching frequency of the semiconductors. To overcome the above difficulties, the association of a switching assistance circuit 'SAC' within the conventional Boost converter is designed. The proposed technique is simple, flexible, accurate, and efficient and the performance of the proposed approach is evaluated by comparing it with the conventional one (without 'SAC' circuit). The obtained simulation results show the effectiveness of the proposed technique in terms of volume minimization and switching losses.

Keywords: DC/DC boost converter, switching loss, 'SAC' circuit, filters, metal–oxide–semiconductor field-effect transistor (MOSFET)

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1. Introduction

Energy converters suffer from power losses caused by transistors; main components of these losses [1] - [4].

One way of limiting power losses in metal–oxide–semiconductor field-effect transistor (MOSFET) transistors is to minimize the blocking time by reducing the gate resistance [5], [6]. Thus, the gate resistance depends on the fan-out of the control circuit and the cut-off frequency of the low-pass filter formed by this resistance Rg and the capacity CGS of the MOSFET [9], [7], [8]. Reducing the gate resistance of the MOSFET can lead to a false interpretation of the measurement results of the switching energy losses based on the form of the drain-source voltage VDS and the drain current ID [9], [10].

This article provides a detailed description of the power MOSFET switching process, considered as the weak link in energy converters. With the use of a switching assistance circuit based on the delay in the rise of the current ID passing through the transistor at the opening (during T_{on}) and delaying the rise of the voltage VDS at the closing (during T_{Off}) (see Figures 2 and 3 *infra*), we have come to lower the energy dissipated by the semiconductor.

During the switching process, the dissipated energy is crucial; the correct determination of its value is quite difficult due to the limitations of experimental measurements. Therefore, the use of an advanced simulation program is useful; to measure the phenomena of energy losses dissipated by the transistor considered in this article, we used the simulation results of the switching process carried out with OrCAD PSpice. These results have been verified by laboratory tests aimed at ensuring their proper functioning under static and dynamic conditions, including the consistency of energy losses measurement dissipated by the Boost converter and the dependency of the output current losses on the duty cycle and frequency.

The rest of this paper is arranged as follows:

Section 2 presents the basic structure of a DC-DC Boost converter.

Section 3 specifies a brief idea on the switching power losses.

In section 4, switching power losses during conduction and blockage are analysed and discussed.

The minimization of transistor switching losses for both cases, during conduction and blockage is developed in section 5.

Combination of assistance circuits in the Boost converter to minimize the loss of energy in switching is presented in section 6.

The experimental and simulation results are provided in section 7.

Finally, the conclusion is presented in the last section.

2. Basic structure of a DC-DC boost converter

The basic structure of a Boost converter is shown in Figure 1, it results from the association of a controlled switch (T) and antiparallel diode (D).

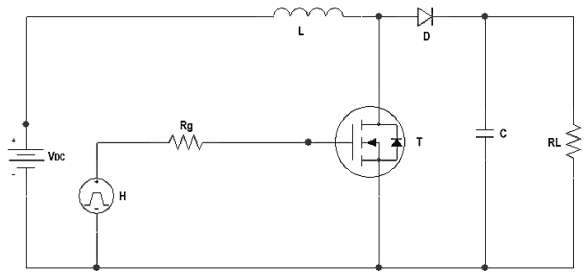

Figure 1. Basic structure of a DC-DC Boost converter

A continuous source (VDC) assumed to be perfect to which a high value capacitor is associated in parallel and acting as a current reservoir feeds the whole. This circuit has two modes of operation depending on whether the current flowing in the inductance L is or is not continuous (does not cancel during the period).

As the continuous conduction mode is the most interesting for this converter, we will only study this mode.

During 0<t<αT:

Transistor T is closed (saturated) and diode D is blocked, we have:

$$V_{DC} = \mathrm{L}\frac{\mathrm{di}}{\mathrm{dt}} \quad (1)$$

from where

$$i(t) = I_{min} + \frac{V_{DC}}{L}t \quad (2)$$

At the instant t = αT the current in the inductance reaches the peak value:

$$I_{Max} = I_{min} + \frac{V_{DC}}{L}\alpha T \quad (3)$$

During αT <t<T:

At t = αT, Transistor T is blocked and diode D becomes conductive and we have:

$$V_{DC} - V_S = L\frac{di}{dt} \quad (4)$$

$$i(t) = I_{Max} - \frac{V_S - V_{DC}}{L}(t - \alpha T) \quad (5)$$

At t = T the current in the inductance reaches its minimum value:

$$I_{min} = I_{Max} - \frac{V_S - V_{DC}}{L}(1 - \alpha T) \quad (6)$$

Let *ΔI* be the ripple of the current in the inductance:

$$\begin{cases} \Delta I = I_{Max} - I_{min} = \frac{V_{DC}}{L}(\alpha T) \\ \quad = \frac{V_S - V_{DC}}{L}(1 - \alpha T) \end{cases} \quad (7)$$

So,

$$V_S = \frac{V_{DC}}{(1-\alpha)} \quad (8)$$

It can be seen that the output voltage of the converter only depends on the voltage input and the duty cycle α. As α is always between 0 and 1, the converter is always a voltage booster.

Note that the output voltage is theoretically independent of the load. In the practice, the regulation loop will therefore only have to compensate for variations in the input voltage and imperfections of the actual components. The most obvious regulation strategy is pulse width modulation (PWM).

When the output current IS decreases, for example by increasing the resistance R_L, the circuit can pass into discontinuous conduction (the current is cancelled during the period).

We show that the expression of the output voltage is then written:

$$V_S = V_{DC}\left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{R_L T}{2.L}\alpha^2}\right) \quad (9)$$

Note that the output voltage is no longer independent of the load and the frequency. It is therefore important to know the operating limit in continuous conduction

3. Measurement of power losses

The measurement of power losses in switches is of great importance for the design of power electronics systems. A method described in [12], [13] consists in taking the current passing through a switch and the voltage at these terminals, in order to find the losses of energies by the product current voltage.

These losses can be defined as the sum of conduction losses, blocking losses to which the switching losses are added.

$$P_T = P_C + P_B + P_{Sw} \quad (10)$$

where:

- P_T: total power dissipated by the switch;
- P_C: power dissipated by the switch during conduction;
- P_B: power dissipated by the switch during blocking;
- P_{SW}: power dissipated by the switch during switching.

The conduction losses and blocking losses are proportional to the square of the current, and for these to be minimized one can use MOSFET switches with:

RDS_{on}<Some *mΩ* in conduction;

RDS_{off}> Some *MegΩ* at blockage.

Where:

RDS_{on}: source drain resistance during conduction;

RDS_{off}: source drain resistance during blockage.

The switching losses change as a function of the switching current, voltage and frequency. To separate these two types of losses, the same operating point, current and voltage is simulated for different frequencies. Measurements by simulation have shown that the variable part with frequency is a linear function, which makes it possible to define the switching energies as:

$$P_C = F.E_{Sw} \quad (11)$$

where:

F: is the switching frequency, the choice of its value is a compromise between the minimization of switching losses and the sizing of the converter, but generally the value of f must be greater than *20 kHz*.

Figures 2 and 3 represent the simulation results of a Boost converter.

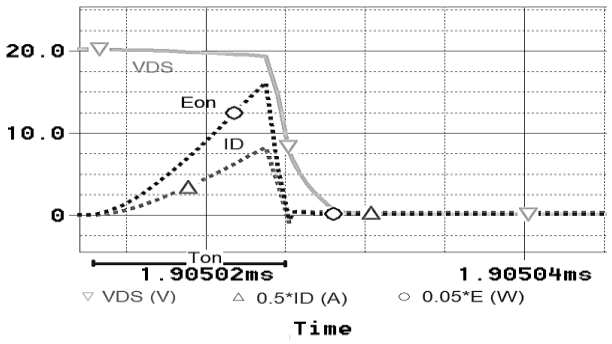

Figure 2. Waveforms of the ID current, the VDS voltage and the dissipated power by the MOSFET during conduction

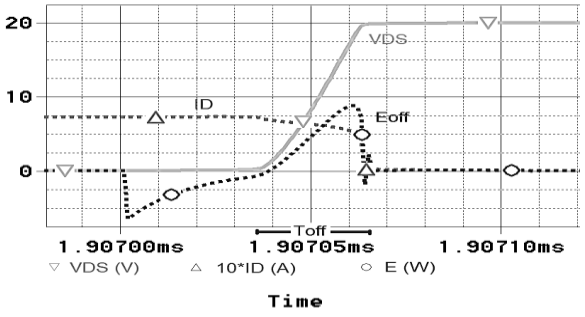

Figure 3. Waveforms of the ID current, the VDS voltage and the dissipated power by the MOSFET during blockage

The simulation was carried out with the following parameters:

Switch *T* = Transistor type MOSFET (IRF640);
Inductance L = *200μH*;
Grid resistance Rg = *20Ω*;
Input DC source VDC = *12V ;*
Load Resistance RL = *50 Ω*.

We can immediately see the presence of peaks of large current during the closing phase (saturation of the transistor T), which can lead to the breakdown of the transistor, this probability increases with the switching frequency.

We note from Figure 3 (*supra*) the presence of peaks of energy dissipation by the transistor during the closing phase, this energy is dissipated in the form of Joule losses therefore, the evacuation of this energy by adequate dissipators is necessary.

4. Switching power losses

The measurement of switching power loss is of great importance for the design of power electronics systems. A method described in [12]-[14] consists of taking, during the switching, the current passing through a switch and the voltage at his terminals and use the product current voltage in order to find the switching energy losses.

The behaviour of the system during blockage is significantly different from that of conduction. Therefore, it is wise to study each case separately in order to quantify the losses during conduction and during blockage. When implementing the SAC to the basic DC-DC Boost converter power losses in this improved converter are compared separately with those of the basic one. This is made, in order to observe the effectiveness of the improved booster during conduction (T_{on}) as well as during blockage (T_{off}).

4.1 Switching power losses during conduction

The nature of the commutations results from the association of a MOSFET transistor and a diode, and from the speed of evolution of the current imposed by the MOSFET (Figure 2, *supra*).

This operation results in switching losses [8], [13] when the MOSFET is saturated:

$$\begin{cases} P_{on} = mean(VDS.ID) \\ \quad = F.\int_{T_{on}} VDS.ID\,dt \\ \quad = F.E_{on} \end{cases} \tag{12}$$

$$E_{on} = P_{Total} - 5.[RDS_{on}(ID_{rms})^2] \tag{13}$$

$$ID_{rms} = \sqrt{F\int_{T_{on}} ID^2(t)dt} \tag{14}$$

where:
P_{on}: Power dissipated by the MOSFET during the conduction phase;
F: The switching frequency applied of the MOSFET;
T_{on}: Rise time of the ID current to which the VDS fall time is added;
E_{on}: Dissipated energy in the switch;
P_{Total}: Total power required by the MOSFET;
RDS_{on}: Source drain resistance during conduction.

It is to note that peak power dissipation is emphasized by the VDS voltage delay to the command TON and the abrupt rising ID current if this delay is reduced peak power dissipation will be reduced considerably.

4.2 Switching power losses during blockage

The rapid deactivation of the MOSFET is a serious problem for anyone designing converters. One method described in [15], [16], [17] consists of using a very low gate resistance Rg in the control circuit, which allows rapid discharge of the input capacitor Ciss of the transistor, through the gate resistance.

Consequently, a large impulse current IGS is observed and this can lead to a breakdown of the MOSFET, or to the destruction of the limited outgoing control circuit. Thus, the rapid deactivation of the MOSFET can be done by the application of a negative voltage, through a push-pull assembly, which allows a very rapid discharge of the input parasitic capacitance Ciss of the MOSFET [8], [18].

The push-pull assembly is built around two bipolar transistors T_1 and T_2 as shown in Figure 8 (*infra*), or two small signal MOSFET transistors. In this latter case it is advisable to choose a pair of transistors with very low RDSON because this will act as a short circuit for the capacitance Ciss during its discharge.

When bipolar transistors are used as push-pull driver T_1 acts as the direct driver of the MOSFET gate during the positive phase of the PWM command pulse which must have a sufficient level to drive the MOSFET into

saturation. Whereas in the null phase the of the PWM pulse T_2 is polarized by the Ciss voltage at the gate and acts at the same time as its discharge circuit.

A faster discharge scheme is obtained when the collector of T_2 is negatively polarized, but this has a drawback of using an additional negative supply in the system.

By following the same steps, we can calculate the power loss during blockage.

$$\begin{cases} P_o = mean(VDS.ID) \\ \quad = F.\int_{T_{off}} VDS.ID\,dt \\ \quad = F.E_{off} \end{cases} \quad (15)$$

$$E_{on} = P_{Total} - 5.[RDS_{on}(Is_{rms})^2] \quad (16)$$

$$ID_{rms} = \sqrt{F\int_{T_{off}} Is^2(t)dt} \quad (17)$$

where:
T_{off}: Fall time of the ID current to which the VDS voltage is added;
E_{off}: Energy dissipated in the switch;
Is:Output current.

As shown in Figure 3 (*supra*), the peak power loss is due mainly to the current *ID* which is delayed relative to T_{off}. In order to reduce this loss, it is best to have a rapid fall time of the current *ID*.

The power losses change as a function of the voltage, current and the switching frequency. To separate these two types of losses, i.e. conduction and switching losses, the same operating point, current and voltage is simulated for different frequencies. The measurements by simulation have shown that the variable part with frequency is a linear function, which makes it possible to define the switching losses as [12]:

$$\begin{cases} P_{SW} = P_{on} + P_{off} \\ \quad = F.(E_{on} + E_{off}) \end{cases} \quad (18)$$

where:
F: is the switching frequency, the choice of its value is a compromise between the minimization of switching losses and the sizing of the converter, but generally, due to electromagnetic compatibility (CE) constraints [14], the value of *F* must be greater than 20 kHz

5. Minimization of transistor switching losses

As we have seen in Figures 2 and 3, the waveforms of the drain ID and the energy dissipated by the MOSFET have peaks. This phenomenon appears when the switching frequencies show natural resonances and especially when the load is inductive or capacitive. These peaks dangerously affect the MOSFET and there is a risk of its destruction at any time. Thus, using the switching assistance circuits to reduce the di/dt or dv/dt is the most adequate solution to remedy the problem.

In order to reduce the loss of energy in switching of the MOSFET, we must slow down the rise of the ID current until the VDS voltage is negligible during the conduction phase and delay the rise of the VDS voltage until the ID current is zero during the blockage phase.

This is accomplished by the implementation of the Switching Aid Circuit in the circuit of the basic DC-DC Boost converter as will be detailed in the following sections.

5.1 Minimization of switching losses during conduction

For switching losses, the transition phases corresponding to the opening and closing of the component cannot be approached in the same way. Indeed, the use of different combinations of loss calculation approximation models, and approximations in the identification of parameters, lead us to large errors in the prediction of power losses. This can have a significant impact on the choice of components making up the converter and on the approach to design objectives regarding energy efficiency and reliability [3].

Semiconductors are responsible for the majority of losses in a converter. The loss calculation mechanisms for these devices are not easy to implement because, as simple as their topology, they are inserted in a highly non-linear environment, so these losses depend on several parameters such as:

- The converter topology;
- The control mode (hard/soft switching);
- Input and output impedances;
- The semiconductor family (MOSFET, bipolar);
- The semiconductor technology used;
- The control circuits;
- The modulation method used;
- EMC constraints (electromagnetic compatibility);
- Thermoelectric couplings;
- Mechanical constraints.

The switching losses are due to the conduction and blocking phases, since the current as well as the voltage must vary over a large range, to reach the magnitudes imposed by the sources between which the converter is inserted. To reduce the switching losses we must, during the closing phase of the MOSFET, slow the rise of the current ID until the voltage VDS is zero or negligible. This is obtained by inserting an additional inductor L1 between the main inductor L and the Drain of the MOSFET as shown in Figure 4.

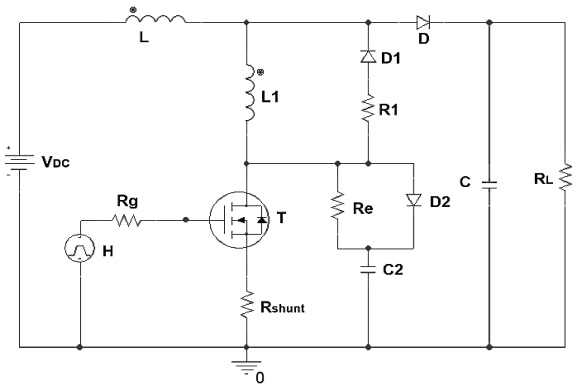

Figure 4. DC-DC boost converter assisted in conduction and blockage (SAC Boost converter)

The inductance L1 behaves like a delay line whose value is calculated by:

$$L_1 < \frac{\alpha.T.r}{5} \quad (19)$$

where:

r: internal resistance of inductor L1;

α: the duty cycle;

T: switching period.

In order to protect the MOSFET during blockage it is necessary to discharge inductor L1 during the phase of blockage. This is obtained by the insertion of a free-wheeling diode D1 and a limiting current resistor R1. This resistor should satisfy the relation:

$$5.\frac{L_1}{R_1+r} < (1-\alpha)T \quad (20)$$

The measurements made on the virtual prototype assisted at the blockage are given in Figure 5, on which we observe:

- The current peaks have become less important, where they go from 20 A to 1 A;
- The peaks of the energy dissipated by the MOSFET are reduced by a factor of 34 (passage from 520 w to 15 w);
- A reduction in Ton closing time by a factor of 6 (from 60 ns to 10 ns).

5.2 Minimization of transistor switching losses during blockage

To minimize the loss of energy during the blockage we connected a capacitor C_2 in parallel with the MOSFET as shown in Figure 4.

This capacitor must maintain a voltage across the terminals DS of the MOSFET during the opening phase only; for this, we insert a resistor R_2 with capacitor C_2; this resistance must be large in one direction which is when the MOSFET is blocked and this is the discharge phase through R_2 where, D_2 is blocked. This resistance must be small in order to permit a rapid charge of C_2 and this is when the MOSFET is conducting. During the charge phase D_2 is conducting and thus bypasses R_2. It is to note that fast diodes should be implemented in the design otherwise the aid circuit may not function and heat may generate from the diode and could lead to its breakdown. In principle, these assisted switching do not generate energy losses. The capacitor C_2 behaves like a delay line for the rise of the voltage VDS, the value of which is determined while respecting the following inequality:

$$5.R_2C_2 < (1-\alpha)T \quad (21)$$

where:

α: the duty cycle;

T: switching period.

The resistor R_2 serves to limit the discharge current of C_2 through the MOSFET in a sense, so the diode D_2 allows the rapid charging of C_2 during the opening of T.

The simulation results are illustrated in Figure 5, in which we note a delay in the rise of the VDS voltage with a decrease in the ID current and the energy dissipated during the blockage phase.

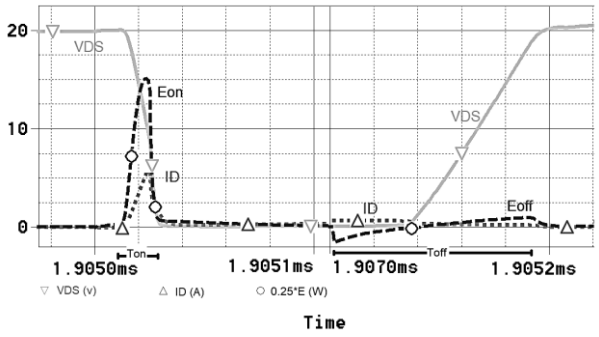

Figure 5. Waveforms of the ID current, the VDS voltage and the dissipated power by the MOSFET during conduction and blockage

6. Combination of assistance circuits in the Boost converter

Finally, and to minimize the loss of energy in switching, for the conduction and blockage phases, we have combined the aid to switching circuits for conduction and for blockage in order to obtain the circuit of Figure 4. The presented circuit is the assisted Boost converter that is practically realized. It is to note that, in practice the aid circuit for conduction implemented in the basic converter functions only during the conduction phase. Similarly, the aid circuit for blockage works only during the blockage phase. The independence of these aid circuits has been of great help during the simulation phase as well as during the practical implementation phase especially for the measurements.

7. Experimental results

In conventional switching converters, there is a switch to control, and in some cases, it is enough to adjust the duty cycle to adjust the output voltage without having to make any regulation. The control of the DC-DC boost converter resembles in principle the control of conventional converters.

7.1 Realisation of prototypes

The experimental prototypes that we have realized are single-cell DC-DC converters; the first consists of a switching cell and a pair of transistors mounted in Push-Pull to adapt the control signal to the MOSFET transistor.

The second is identical to the first to which is added a switching assistance circuit (SAC).

The first step of the realization consists in determining the switching frequency which facilitates the implementation of the command and control of the conversion cell. The semiconductor power components are dimensioned to limit losses, which depend on switching times, and on the level of high frequency emissions. The choice of driver which allows the adjustment of switching times to act both on switching losses and on the level of emissions. The system must operate in a closed loop to regulate the output voltage. Once the architecture and dimensions of the filter have been defined, we are left with the type of regulation that is required which ensures high bandwidth and system stability in a closed loop.

The voltage across the shunt resistor R_{Shunt} allows the ID current to be measured and to know if it is exceeded,

Since,

$$ID = \frac{V_{DS}}{R_{Shunt}} \quad (22)$$

The measurement procedure automatically reviews the desired points in the current range. The measurement of the losses corresponding to a given current lasts only a few tens of milliseconds [6]. The current points are successively made with a few seconds apart in order to calibrate the temperature of the heatsink [9].

The input and output currents and voltages of the two prototypes are measured and recorded. Each of these tests is performed with the same current and voltage conditions for different switching frequencies. Test data is used to calculate the overall loss of the converters.

The results of these tests are shown in Figure 6, where the power dissipated by the converters has been plotted, the first is assisted at switching while the second is unassisted.

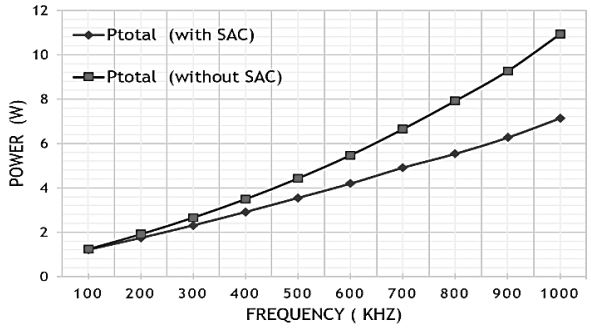

Figure 6. Variation of the total power dissipated by the Prototypes as a function of the frequency

We can see that the shapes of the curves, of the powers dissipated by the two converters, are almost linear.

Thus, the total energy dissipated by the prototype is: E = 5 W for the assisted converter and E = 11 W for the non-assisted, that is to say at a switching frequency of 1 MHz the assisted converter will dissipate an energy of 6 W less than the unassisted converter and this represents 45 % of the energy dissipated by the non-assisted converter.

7.2 Measurement of switching losses

The measurements of losses in the power switches are carried out using a method inspired by the method of "double pulse" [2] used generally for Thyristor switching. Two methods are used for this purpose.

The first one consists of applying a positive pulse to the gate of the blocked MOSFET until the VDS voltage is null then immediately the MOSFET is blocked again. The measured dissipated energy during this short time is mainly due to switching because the blockage energy is negligible [14].

The second consists of driving the MOSFET by a pulse whose width is equal to the sum of Ton and Toff. The measured dissipated energy during this short time is due mainly to switching since the blockage energy is negligible [15]. It is to note however that both methods give the same results and that all the timings Ton, Toff are taken from the simulation results shown in Figures 2, 3 and 5.

However, there are some drawbacks to these methods.

On one hand, a current probe must be inserted in the switching mesh which increases the mesh inductance, the overvoltage and the losses themselves.

On the other hand, the probe must be calibrated, compensated and have a very high bandwidth.

Finally, if the integral of the VDS • ID product over a period of the system represents the dissipated energy, this product is over a more restricted and arbitrary interval.

We note that the shapes of the curves, of the powers dissipated by the MOSFET switches, are almost linear thus (Figure 7).

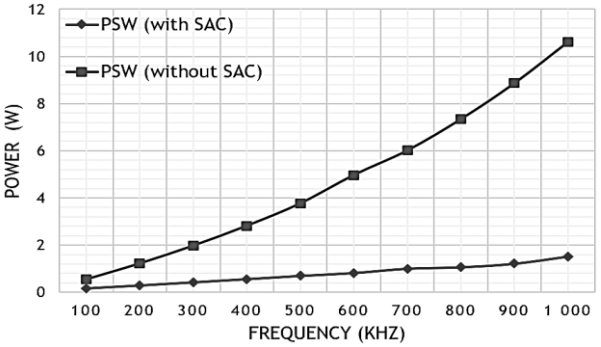

Figure 7. Variation of the power dissipated by the MOSFETs as a function of the frequency

$$P_C = \mathrm{k}.F \quad (23)$$

where:

P_C: is the power dissipated by the MOSFET Switch in the prototype;

K: is a constant value.

By comparison to equation (11) we can deduce that,

$$\mathrm{k} = \mathrm{E_{SW}} \quad (24)$$

Thus, at a switching frequency of 1 MHz, in the non-assisted converter the MOSFET will dissipate a switching power of 10.62 W, on the other hand, in the assisted converter the MOSFET will dissipate a switching power of 1.52 W. This represents only 14 % of the energy dissipated by the non-assisted converter.

In this case, it is seen that in the assisted converter a considerable reduction in size of the switch heatsink is obtained thus allowing a reduction in the volume and weight of the final design.

To measure the switching losses in the prototypes that we have produced, we used a method described in [19], [20], which consist of taking the voltage across a switch, and the current flowing through it during switching, it is possible to find the switching energies by integrating the product current voltage [21].

As mentioned earlier, the current measurement is derived from the voltage across a very small resistor incorporated between the source of the MOSFET and ground [22]. This resistor, (R_{Shunt}) typically has a value on the order of 0.22 ohm.

However, this method requires the use of wide bandwidth, calibrated and compensated probes [18], [23], [24].

In addition, it is very intrusive, due to the addition of parasitic elements in the switching mesh. This can cause voltage overshoots and slowing down of the di/dt, dv/dt, when the values are not adequately chosen.

For low frequencies both prototypes have nearly the same efficiencies, this is due to the fact that rise and fall times of the MOSFET are negligible compared to the pulse command duration. Whereas, at higher frequencies they could be a fraction of that pulse. In addition, one of the main goals of this design is that high frequency boost converter use smaller components (especially inductors) and this would lead to compact designs with higher efficiency.

8. Command and control

To cope with fluctuations in operating conditions and variations in the electrical load, the control of our DC-DC step-up converter must be checked and corrected in real time. Real-time feedback is necessary to compensate for energy losses and variations in input voltage and load, plus compensation for losses due to temperature changes in semiconductors.

8.1 The command signal

The PWM command signal to be applied to the gate of the MOSFET through the push-pull driver must meet the conditions of amplitude and frequency:

- The PWM pulse must have a sufficient amplitude to drive the MOSFET into saturation through transistor T1 which must be saturated as well. In the case where T_1 is not saturated the MOSFET switch may not saturate as well (conduction mode) and this could lead to its destruction at higher currents Figure 8.
- The width of the pulse must be large enough especially at higher frequencies, in order to avoid overlapping of the front edge of the pulse with the rise time of the switch defined by the manufacturer.

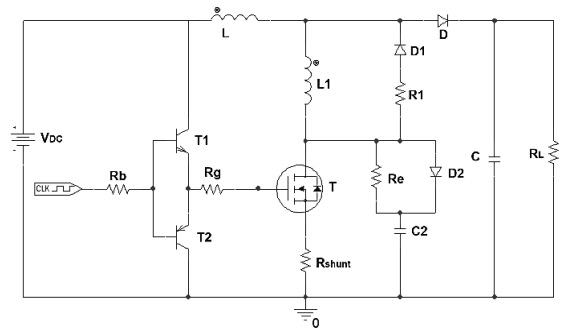

Figure 8. Schematic of the DC-DC Boost converter with its switching assistance circuit and its push-pull driver

8.2 The Controller

The control algorithms described in this section correspond to steady state operation. Two control techniques have been developed:

8.2.1 Classic control (PWM)

In this part we applied a PWM command to our switching cell. The control signal has a duty cycle α. The voltage delivered by the switching cell is a contained voltage with a value very close to the one indicated by equations (8) and (9).

This algorithm is characterized by:

- Convergence time is variable;
- Convergence time proportional to the pre-set voltage value;
- No overshoot of the output voltage Vs.

8.2.2 Proposed control

This algorithm is deduced from the method of numerical resolution of linear equitation's known by the Dichotomy algorithm.

This algorithm is characterized by:

- Short convergence time;
- Convergence time does not depend on the pre-set voltage value;
- Presence of excess voltage Vs (overvoltage).

9. Conclusions

This work is dedicated to determining the switching losses of power MOSFETs in order to minimize them. These losses were simulated by OrCAD-PSpice simulator. These simulations allowed us to mathematically model the switching losses of semiconductors with a specified switching mesh. The sensitivity of the model for certain parameters has been verified with waveforms described in the literature. Oscillations at the beginning and at the end of the commutations were observed.

These oscillations modify the waveforms, but they do not generate significant losses. The study of the parasitic elements studied here allowed us to draw some fundamental conclusions: An increase in the negative gate voltage has a negative impact on the overshooting of the VDS voltage during the blocking of the Transistor. However, this voltage also increases the driver's noise immunity, thus avoiding unwanted reboot of the component.

It is clear from the experimental results that, the SAC Boost converter performs better than the basic converter in all the frequencies above 100 KHz, while both converters have the same efficiency below 100kHz. Because of the high frequency, the SAC converter is designed with reduced size and weight components thus allowing compact designs with minimum thermal relief and hence higher efficiency.

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