Signal Analysis-based Diagnosis Method for Multi-Level Flying Capacitor Converter under Open-Circuit Fault

Thiziri BEN ALI[1], Abdellah KOUZOU[1], Ahmed HAFAIFA[1], Ali TETA[1]

[1]Applied Automation and Industrial Diagnostics Laboratory (LAADI), Djelfa University, Algeria, University Ziane Achour of Djelfa, Algeria

Abstract

Multi-level inverters have become widely used in several high and medium power applications owing to their improved output voltage compared with the output voltage provided by two level inverters. However, when a fault occurs in a cell in the converter it could lead to a failure or malfunction on the application chain of the whole system. Therefore, automatic failure detection is becoming more and more essential. In this paper, a new algorithm is developed for switch open-circuit fault detection and localisation in a flying capacitor multilevel converter. The proposed algorithm is not dedicated only for the fault detection, but also for faulty switch localization. Since the output voltage of the FC converter is totally related to the control applied on the switches, the proposed technique requires only the output voltage and pulse width modulation (PWM) switching signals. A mathematical model is developed to provide a reference signal for all the considered faulty cases. Next, the faulty switch is precisely located after performing a procedure through several comparators and filters. This paper aims first to provide detailed explanation of the proposed algorithm, followed by a validation through an extensive simulation and finally the analysis of the results, which confirm the performance of the proposed technique.

Keywords: multilevel inverters, flying capacitor converter, pulse width modulation (PWM),open-circuit fault, fault detection

Received: 28 January 2020

To cite this article:
BEN ALI T., KOUZOU A., HAFAIFA A., TETA A., "Signal Analysis based Diagnosis method for Multi-level Flying Capacitor Converter under Open-Circuit Fault", in *Electrotehnica , Electronica, Automatica* (*EEA*), 2020, vol. 68, no. 1, pp. 12-20, ISSN 1582-5175.

1. Introduction

In high voltage applications, the use of conventional inverters that provide two output levels is limited due to the switching losses and constraints of device rating [1].

To overcome the drawbacks of conventional two level inverters, a new topology has been introduced in early 1975[2], namely, *multi-level converters*.

The introduced topologies are easily able to convert DC voltage from a continuous source such as a battery or photovoltaic system into a multi-level AC voltage waveform. These inverters are used for the purpose of adjusting the speed of rotation in motor drives [3–5], avoiding the loss of information in case of power failure in UPS (Uninterruptible Power Supply) systems and ensuring the energy transfer between two different frequency networks in power system drives. Currently, their use has been increased in industry, especially in high voltage applications, where a high level of reliability must be ensured [6, 7].

To generate a multilevel voltage, different structures have been proposed, such as the Neutral point clamped multilevel inverter (NPCMI), the Flying capacitor Multi-level Inverter (FCMI) and the Cascaded H-Bridge Multi-level Inverter (CHBMI) [8]. As the number of levels increases, the output signal approaches to the sinusoidal form, which has a reduced harmonic distortion [9]. One of the major characteristics of these converters is that they can operate with a very low switching frequency, therefore reduced switching losses [10].

To control these converters, several control strategies have been developed, including sinusoidal pulse width modulation (PWM), selective harmonic elimination and space-vector modulation (SVM), etc.

The reliability of the converters is a crucial factor, since a fault in these circuits may provoke a failure or malfunction over the entire application chain in case of no fault-tolerant strategy is used[11].

The present paper focuses mainly on flying capacitor multi-level inverter based on the use of Insulated Gate Bipolar Transistors (IGBTs). Indeed, faults in IGBTs can be classified into three types [12-13]. The open-circuit faults lead to a significant degradation and distortion in the output current and voltage, hence a non-symmetrical waveform results within the output current and voltage. In this case, an immediate shutdown is not required, but it degrades the performance of system [14-15]. Contrariwise, the short-circuit faults (or transistor latch-ups) can cause several damages due to the overheating of IGBTs [16], this will affect the other components and lead to complete failure [17]. The third type is intermittent gate-misfiring faults, this kind of faults leads to a degradation and malfunction of the applied control strategy [15].

Two main types of strategies are adopted for fault detection.

Firstly, the quantitative diagnosis that requires the use of a mathematical model like the parity space, parameter estimation method and observers based method. There are also some methods based on signal processing techniques such as filtering, thresholding and spectrum identification approaches, where in the residues, which is the gap between the estimated and measured outputs, is highly needed.

Secondly, the qualitative diagnosis that is based on data exploitation such as Pattern Recognition and artificial intelligence methods [18].

In recent years, many strategies have been proposed in the field of fault detection in IGBTs.

In [19], a technique is proposed to single out the short circuit of a cell based on the vector analysis of the output phase voltage.

In [20], a model-based predictive control was developed for the purpose of singling out the faults of short circuit and identifying the failed switches. However, to perform the detection using this method, a complicated and huge calculations are required, on the other side, the voltage level of the healthy case will not be ensured in case of fault occurring. Therefore, this technique has two main drawbacks, the limitation of the protection speed and the limitation of its application for multilevel inverters.

In [21], the author uses a detection method based on sliding mode observer where the open circuit faults can be located. However, its performance is limited when the systematic measurement error is higher than 7%.

In [22-23], a detection approach based on analysing the switching frequency component of the output phase voltage in FC converter was proposed. This method is able to identify the faulty cell. However, the faulty switch cannot be located in addition to the complication of the used algorithm.

In [7], the authors proposed to involve the artificial intelligence to detect the faults in cascaded H-bridge.

In [24], a fuzzy logic-based technique was used to find out the faulty switches in the inverter for induction motor drives, although the good performance of these two last methods, they require long computation time to ensure the diagnosis process.

In [11], a fault-diagnosis and fault-tolerant control scheme were proposed by using the charging state of capacitors and the applied switching states.

In [25] and [26], an algorithm based on analysing the inverter switching signals besides the line-to-line voltage is proposed.

In [27], a fault detection and an isolation technique was proposed by comparing the measured pole voltage with the estimated pole voltage obtained from the mathematical model. These methods provide a fast response compared to other methods. However, they were applied only for two level inverters.

One of the major drawbacks in the aforementioned methods is the need to a complicated mathematical model in all the methods, which is quite difficult to obtain, and it can be inaccurate in case of switching devices-based system. On the same time, these methods require an extensive computation and a long time diagnosis due to the used data processing approaches.

In this paper, we have modified the mathematical equation of the converter in its normal state to obtain the defective converter model. As the open-circuit fault occurs due to the disconnection of an IGBT, the control signal of each cell in the proposed equation must be neglected to model the fault in the same cell. Thus, a comparison will be performed after a signal processing for the output signal of the converter and the estimated output calculated by the equations to locate the fault. The comparison between the two extracted signals provides information on the defective switch. The proposed strategy overcomes several limitations in the aforementioned methods, so that it does not require an observer or complicated calculations.

The rest of the paper is constructed as follows: in the first section, a review on the flying capacitor multi-level inverter (FCMLI) structure is presented with its mathematical model and then the PWM technique that is used for the control of the switches of the studied multi-level inverter is explained in details. The next section focuses mainly on the proposed fault detection method. The third section presents the simulation performed for the validation of the proposed algorithm, where the obtained results are illustrated and discussed. Finally, the conclusion.

2. Multi-cell converter topology descriptions

Flying capacitor multi-cellular converters appeared in the early 1990s, following a patent presented by Maynard and Foch [28]. This topology did attract considerable attention by many researchers and industries due to the inherent property of natural voltage balancing. Indeed, this topology has a main feature that it allows splitting the input voltage among the cells following precise percentage and hence clamping the voltage stress across the used switches [29].

In this modular topology, only one DC source is needed: (n-1) floating capacitors and n pairs of switches forming the cells, which are connected in series to generate (n + 1) output voltage levels, as shown in Figure1A).

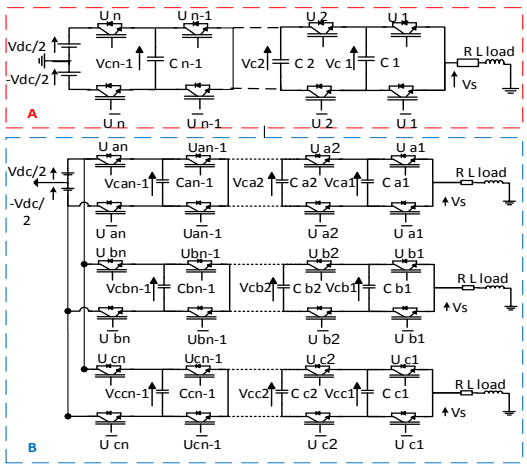

Figure 1. General structure of a multi-cellular N-level inverter: A) single phase; B) three-phase

On the other side, it does not require any clamping diodes and it can operate without snubber circuits [30]. In this topology, the switches pairs are considered as cells, between which floating voltage sources are interleaved by means of capacitors [31].

The general structure of the multi-cellular three-phase converter (FC) is shown in Figure 1B). The architecture of the multi-cell converters has a modular structure that allows improving the waveform quality of the output voltage of the converter by increasing the number of levels without increasing the switching frequencies [32].

It can be said that this topology ensures an output waveform voltage who's a fundamental that follows accurately the reference output voltage. In addition, it offers the advantage of obtaining a reduced amplitude spectrum, hence less ripples in the output voltage, this is explained by the obtained THD which is minimized remarkably [32].

At the terminal of all the switches, the blocking voltage is the same. It has also the advantage of decrease of the stresses on switches.

This structure is able to operate as a chopper or inverter in full bridge or half bridge.

2.1. Mathematical model

The switches are considered ideal, so the switching time is zero, and the supply voltage V_{dc} is constant.

For a multi-cellular inverter with n cells, the voltage between each cell can be expressed as follows:

$$V_{Cell\ j} = V_{Cj} - V_{Cj-1} \tag{1}$$

For $j = 1, \dots, n$

where:

$$\begin{cases} V_{c0} = 0 \\ V_{cn} = V_{dc} \end{cases}$$

The capacitor voltage can be obtained by the following equation:

$$V_{cj}(t) = V_{cj}(0) + (u_{j+1} - u_j)\ \frac{1}{C_j}\int i_s\, dt \tag{2}$$

where:

u_j: the stat of the switch j, and

$$\begin{cases} u_j = 0\ , (j : opened), \\ u_j = 1\ , (j : closed). \end{cases}$$

C_j: The capacitor$j$

i_s: The output current.

The output voltage can be expressed by the following equation:

$$V_s = \sum_{j=1}^{n}(V_{Cj} - V_{Cj-1})u_j \tag{3}$$

At steady state:

$$\begin{cases} V_{cj} = j\frac{V_{dc}}{n} for j = 1, \dots, n \\ V_{cell} = \frac{V_{dc}}{n} \\ V_s = \lambda\frac{V_{dc}}{n} \text{ where } \lambda = \sum_{j=1}^{n} u_j \end{cases} \tag{4}$$

The behaviour of the inverter can be presented by the following equations:

$$\begin{cases} \dot{V_{c_j}} = \frac{u_{j+1}-u_j}{C_j} i_s \\ \dot{i_s} = \frac{u_{j+1}-u_j}{L} i_s\ - \frac{R}{L} i_s + \frac{V_{dc}}{L} u_{j+2} \end{cases} \tag{5}$$

Taking into account that the load is RL and the structure is in half bridge, the output voltage can be expressed as follows: [33]

$$V_{ch} = V_s - \frac{V_{dc}}{2} = Ri_s + L\frac{d}{dt} i_s \tag{6}$$

Equation (7) gives the evolution of the current i_s, which can be expressed as follows:

$$\frac{\mathrm{d}}{\mathrm{dt}}\mathrm{i_s} = \frac{\mathrm{V_s}}{\mathrm{L}} - \frac{\mathrm{R}}{\mathrm{L}}\mathrm{i_s} - \frac{\mathrm{V_{dc}}}{2\mathrm{L}} \tag{7}$$

2.1.1. Sinusoidal Pulse Width Modulation control

The PWM pulses are generated by the comparison between the sinusoidal modulus wave $R(t)$ and the triangular wave $T_{r_n}(t)$ (or Sawtooth) where their intersections present the switching instants, as shown in Figure 2.

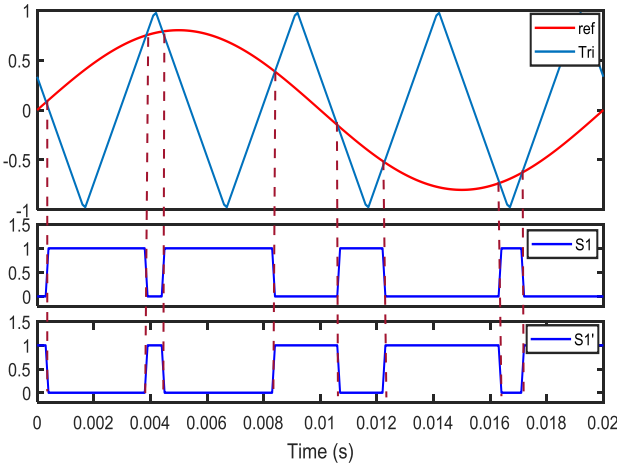

Figure 2. Principle of the sinusoidal PWM control

It is worth mentioning that the frequency of the Sawtooth signal must be higher than the frequency of the reference signal $R(t)$ [11].The frequency of the reference signal determines the frequency of the output signal.

$$u_j(\mathrm{t}) = \begin{cases} 1, R(t) \geq T_{r_n}(t) \\ 0, R(t) < T_{r_n}(t) \end{cases} \tag{8}$$

$$R(t) = A_r\ sin\ 2\pi F_r t \tag{9}$$

where A_r, and F_r are the amplitude and frequency of the reference signal.

The carrier signal $T_{r_n}(\mathrm{t})$ is defined by [33-36].

$$T_{r_n}(\mathrm{t}) = A_c\ (\tfrac{1}{2} + \tfrac{1}{\pi} arcsin(\sin\ (2\pi F_c t - \varphi_{\mathrm{n}}))) \tag{10}$$

where A_c and F_c are the triangular carrier amplitude and frequency respectively.

Remark: switching frequency is set by the carrier, and the triangular waves must be phase-shift by φ_{n}.

$$\varphi_{\mathrm{n}} = (p-1)\frac{2\pi}{n} p \in 1, \dots, n \quad (11)$$

Frequency modulation rate (m_{f}):

$$m_{\mathrm{f}} = \frac{\mathrm{F_c}}{\mathrm{F_r}} \quad (12)$$

Modulation rate (the coefficient of adjustment (r_{f})):

$$r_{\mathrm{f}} = \frac{\mathrm{A_r}}{\mathrm{A_c}} \quad (13)$$

In order to avoid provoking a short circuit in the inverter switches connected in the same leg, the control signals of each pair of switches must be complementary [31].

For n cells, 2^n different switching states can be configured to control the flying capacitor converter, which is able to generate $\mathrm{n}+1$ voltage levels in steady state.

In three-phase, the three sinusoidal references of the PWM control are phase-shifted by $\frac{2\pi}{3}$ at the same frequency F_r.

The switching states and output voltage of the three cells FC inverter are listed in Table 1.

Table 1. Switching states and output voltage of three cell FC inverter

	u_1	u_2	u_3	$\overline{u_1}$	$\overline{u_2}$	$\overline{u_3}$	V_s
1	0	0	0	1	1	1	$-\frac{V_{dc}}{2}$
2	0	0	1	1	1	0	$-\frac{V_{dc}}{6}$
3	0	1	0	1	0	1	
4	1	0	0	0	1	1	
5	1	1	0	0	0	1	$\frac{V_{dc}}{6}$
6	1	0	1	0	1	0	
7	0	1	1	1	0	0	
8	1	1	1	0	0	0	$\frac{V_{dc}}{2}$

3. Transistor Open Faults Behaviour

The problem of the disconnection of an IGBT from the inverter circuit, caused by gate-driver failure or the lifting of bonding wires (thermic cycling), causes an open circuit fault as shown in Figure 3b) [12], [37].

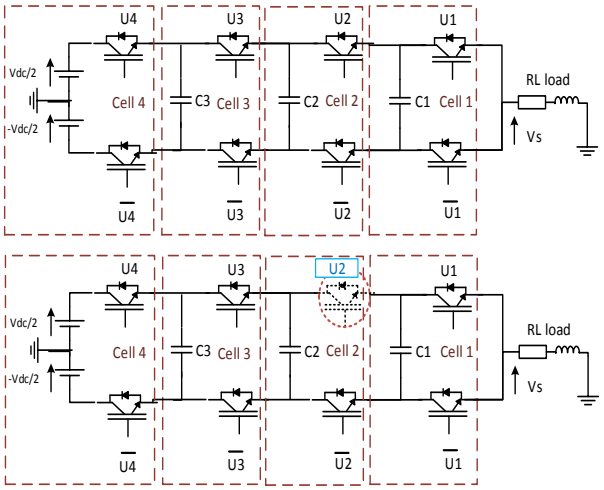

Figure 3. A five-level FC inverter leg: a) normal condition; b) open-circuit fault in the upper switch of the second cell

This fault distorts the shape of the output signal and creates several significant harmonics.

The open circuit fault in the upper switch of any cell, in the flying capacitor converter causes a loss of the positive sign of the output signal part.

Likewise, for the lower switch blocks the negative output signal part. These criteria are a very useful key to locate the open circuit in the upper or in the lower arm.

4. The proposed method for the diagnosis

In this section, we present the principle of the proposed fault diagnosis technique, wherein we will focus more particularly on the open circuit fault. The short circuit fault can cause an explosion. For such reason, a hardware solution is proposed, which can be achieved by insulating the defective switch using a fast-acting fuse or the circuit breakers to pass to the case of an open switch. [24,25].

The output voltage of the inverter and the PWM switching signals are used to perform the fault detection and diagnosis based on their shape.

The output Voltage of the converter V_s results from the choice of n PWM pulses, as can be seen in equation (3), the output voltage is in term of the internal voltage and the control signal. In our diagnosis, we will use another equation that depends only on the control signal.

For n cells inverter, the mathematical model is given by the following equation:

$$V_{r_j} = \left(2u_1 + \cdots + 2u_j + 2u_n - n\right)\frac{E}{n} \quad (14)$$

where:

$$E = \frac{V_{dc}}{2}$$

V_{rj}: the calculated output voltage by the mathematical model.

u_j: the PWM pulses of the switch j, $(j \in 1,..,n.)$.

The open circuit fault can be characterized by an interruption of IGBT control signal. In case, where the

switch j is defective, its control signal u_j is not affecting in any way the output voltage.

Therefore, the other signals are the responsible for controlling the output voltage. Based on this principle, we will modify the equation in normal mode by ignoring the signal corresponding to the defective cell to obtain a defective model, where $u_j = 0$ for a defect in cell j $((j \in 1,..,n.))$.

This method based on comparing the measured output voltage V_s of the inverter and the reference signals V_{rj} obtained from equation (14).

To get the defect mode equation we have to ignore the signal u_j of the switch$j$.

This comparison is performed based on a signal processing process to ensure an accurate comparison where the delay and the magnitude limits are taken into account in this process.

The proposed method has several stages to perform the accurate diagnosis and to ensure the exact identification of the defected switch.

1) $\mathbf{V_s == V_{rj}}$**?**

In the first step, the appearance of the fault can be detected based on the comparison of the measured output voltage of the inverter with the one obtained from equation (14).

2) $\boldsymbol{V_s > 0}$?

The next step is used to determine whether the positive or negative current path that has been blocked to determine whether the fault is in the upper or lower switch based on the identification of the polarity of the measured voltage by comparing the output voltage with zero.

3) After the identifying the whether the default is in the upper or the lower switches, three signal processing tasks is performed in order to precisely localize the defected switch.

Task 1: Extract the sensed envelope

In this task, the required envelope (EDDo) is extracted from the sensed output voltage Vs.

Task 2: Calculate the reference signals

The reference signals ($V_{r1} \ldots . V_{rm}$) for each case of faults are calculated using the mathematical model of equation (14). Therefore, for *n* cell converter we get *n* references signals.

Task 3: Extract the required reference envelope

A processing treatment is performed to extract the required envelop (EDDj) from the corresponding.

Finally, a comparison is performed among the extracted envelopes in order to decide which cell is defected. It is worth mentioning that, by using this method, we can localize the fault and identify exactly which cell is defective.

The operating principle and all the tasks of the proposed algorithm are illustrated in the flowchart (Figure 4).

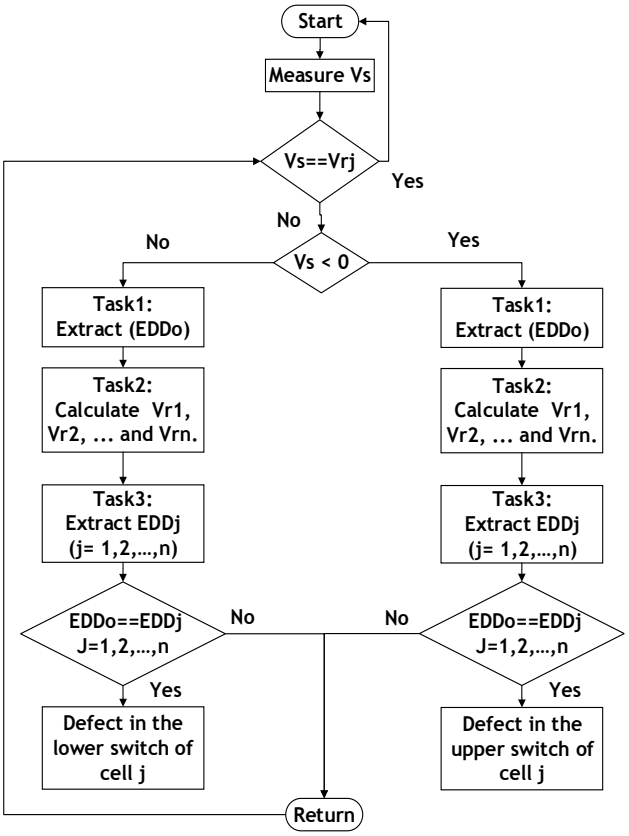

Figure 4. Flowchart of proposed algorithm for the diagnostic

4.1 Algorithm test for five level FC converter

As a first step the proposed diagnosis method will be tested on four-cell flying capacitor converter. All the switching state and obtained output voltage are listed in Table 2.

Table 2. Switching state and output voltage of the 4-cellFC inverter

u_1	u_2	u_3	u_4	$\overline{u_1}$	$\overline{u_2}$	$\overline{u_3}$	$\overline{u_4}$	V_s
1	1	1	1	0	0	0	0	$\frac{V_{dc}}{2}$
1	1	1	0	1	1	1	0	$\frac{V_{dc}}{4}$
1	1	0	0	1	1	1	0	0
1	0	0	0	1	1	1	0	$-\frac{V_{dc}}{4}$
0	0	0	0	1	1	1	1	$-\frac{V_{dc}}{2}$

The output voltage of a four-cell half-bridge converter is described in equation (15).

$$V_s = (2u_1 + 2u_2 + 2u_3 + 2u_4 - 4)\frac{E}{4} \quad (15)$$

where: $E = \frac{V_{dc}}{2}$

The default model of a 4-cell converter is:

$$V_{r_1} = (2u_2 + 2u_3 + 2u_4 - 4)\frac{E}{4} \quad (16)$$

$$V_{r_2} = (2u_1 + 2u_3 + 2u_4 - 4)\frac{E}{4} \quad (17)$$

$$V_{r_3} = (2u_1 + 2u_2 + 2u_4 - 4)\frac{E}{4} \quad (18)$$

$$V_{r_4} = (2u_1 + 2u_2 + 2u_3 - 4)\frac{E}{4} \quad (19)$$

Equations (15) to (19) allow us to characterize the fault in the first cell, the second cell, the third cell and the fourth cell, respectively.

The localization of defect is based on Table 3.

Table 3. Comparison between the output and reference voltages

$V_s < 0$				
Switch in defect	$V_s == V_{r_1}$	$V_s == V_{r_2}$	$V_s == V_{r_3}$	$V_s == V_{r_4}$
u_1	1	0	0	0
u_2	0	1	0	0
u_3	0	0	1	0
u_4	0	0	0	1
$V_s > 0$				
	$V_s == V_{r_1}$	$V_s == V_{r_2}$	$V_s == V_{r_3}$	$V_s == V_{r_4}$
$\overline{u_1}$	1	0	0	0
$\overline{u_2}$	0	1	0	0
$\overline{u_3}$	0	0	1	0
$\overline{u_4}$	0	0	0	1

5. Results and interpretation

To validate the proposed fault detection technique in FC multi-level inverter, simulation tests of five-level multilevel FC inverter topology under healthy and faulty state have been performed using PWM control technique. The signals used for diagnosis obtained by equations (16) to (19) are taken for each case of failure.

The parameters used for simulation are summarized in Table 4.

Table 4. Simulation parameters of the studied flying capacitor multilevel inverter

Parameter	Value
DC Link Voltage(V_{dc})	1600 V
Flying Capacitors	33e-3Uf
Switching frequency	1kHz
Load (R ,L)	R=30Ω L=5e-2 H
Output Voltage frequency	50 z

5.1. Healthy state

The output voltage of the converter in normal mode is shown in Figure 5a), wherein it is obvious that, the inverter provide five levels voltage, as follows:

$(\frac{V_{dc}}{2}, \frac{V_{dc}}{4}, 0, -\frac{V_{dc}}{4}, -\frac{V_{dc}}{2})$.

The output current and the THD the output voltage are shown in Figure 5b) and 5c).

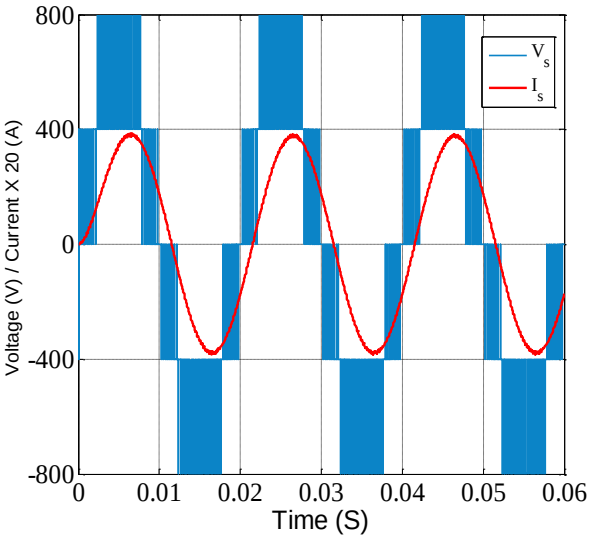

Figure 5. The output voltage of the converter: a) the output voltage; b) the output current; c) THD of output voltage

Before testing the proposed algorithm in the faulty cases, it is activated in the normal mode as shown in Figure 6a) where in it is obvious that once we activate the algorithm at 0.02s it starts extracting the upper and lower envelope from the output voltage.

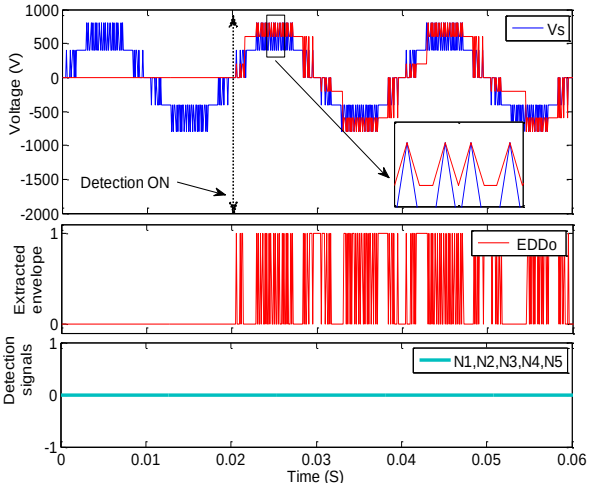

Figure 6. a) Output voltage b) The extracted signal EDDo, c) Algorithm indicators

In the zoom box in Figure 6a), we notice that the envelope coloured in red is following accurately the upper band of the output voltage.

Next, the extracted signal is transformed to a binary signal (EDDo) as shown in Figure 6b).

After, the treated signal will be compared with the reference signal, which is treated using the same mentioned concept.

Since the inverter is operating in its normal mode, there is no output in the indicators of the algorithm, as shown in Figure 6c), where in N1, N2, N3 and N4 are the fault indicators for cell 1 to 4.

N5 is to decide that the fault is in the upper or the lower switch as follows:

0: no fault;
1: fault in the lower switch;
2: fault in the upper switch;

5.2. Faulty state

In this scenario, the proposed algorithm is tested first to detect and locate a fault in the switch located at up in the second cell, as we can see in Figure 7a).

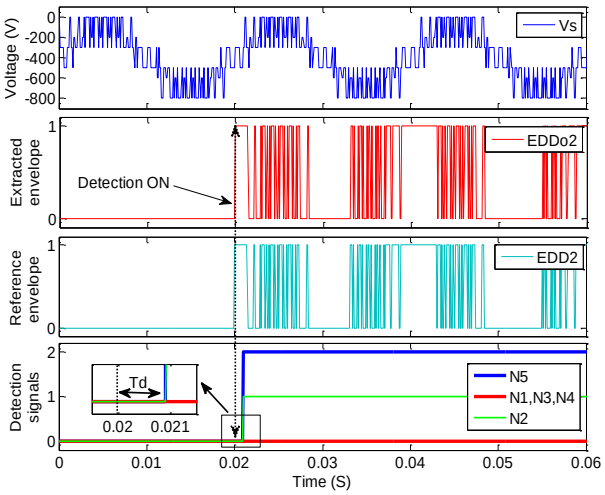

Figure 7. a) Output voltage, b) The extracted signal EDDo1, c) The reference signal EDD2, d) Algorithm indicators

The positive part of the output voltage is eliminated due the faulty conditions.

Figure 7b) demonstrates that, when the algorithm is initialized, it starts extracting the required signals from the output voltage following the aforementioned procedure which is explained in the previous subsection.

Therefore, a binary signal is generated as shown in Figure 7b). There generated signal will be compared with the signal in Figure 7c) in order to perform the detection and the localization.

Once the comparison is in processing, the algorithm plotting the indicators shown in Figure 7d), where we can notice that, the indicator N2 rising from 0 to 1 at 0.021s, which means that the inverter has a faulty switch located in the second cell. While N1, N3 and N4 equals zero because the cells 1, 3 and 4 have nor faulty switches. The fifth indicator N5 is rising to 2 which means that the upper switch in the second cell is defective. It is worth mentioning that, there is a delay Td of 0.001s between the instant of the algorithm activation and the instant of the fault detection.

However, the delay can be minimized using high calculation processors.

The second test is performed under a faulty spot located in the fourth cell in the lower switch.

The output voltage presented in Figure 8a) is distorted and only the lower part is generated because of the fault occurs in the lower switch.

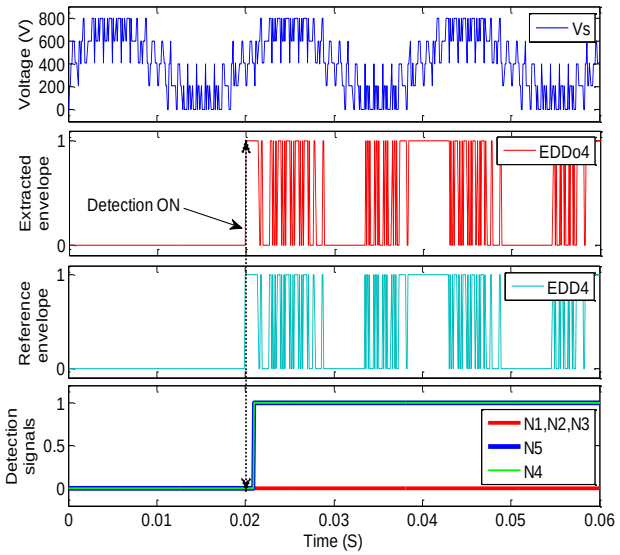

Figure 8. a) output voltage, b) the extracted signal EDDo4, c) the reference signal EDD4, (d) algorithm indicator

At 0.02s the algorithm is initialized and the extracted signal to perform the detection is shown in Figure 8b).

The extracted is further compared with the reference signal to locate the faulty cell.

In Figure 8d), we can easily locate the faulty switch through the results generated by the proposed algorithm wherein the indicator N4 locates the faulty switch which in the fourth cell, while the indicator N5 indicates that the fault is in the lower switch.

By comparing the output voltage in the healthy state of the converter with the signals in faulty state:

- It can be seen that there is a deformation of in the output voltage.
- The deformation is specific for each case of fault. The signal extracted from the system output in case of fault in the first cell matches only to the signal extracted by the first reference, the same for the others fault in case of defect in any switch.
- A half of the output voltage waveform is lost in way if the fault is in the upper switch, only the negative part of the signal remains and even for the fault in the lower switch, only the positive part of the signal remains.

By using the algorithm in the flowchart, we have succeeded to detecting and locating the defect in the converter.

6. Conclusions

This paper provides a detailed analysis of the behaviour of the flying capacitor converter under healthy and faulty situation, where we found that the output voltages carry the default signatures.

A new diagnostic method is proposed for the detection and the localization of open circuit fault in FC converter that applied to a FC converter with four-cell.

The proposed technique is based on the extraction of the envelope of the output voltage and compare it

with the envelope obtained theoretically in order to precisely localize the faulty switch.

On the same hand, the purpose of this method is the diagnosis of defects in FC converter using only the output voltage signal and the pulse-width modulation (PWM) switching signals without the use of additional sensors or observers, which eventually decreases the complexity of the diagnosis operation and reduces monitoring costs.

Through the simulations carried out for the propose of testing the proposed algorithm to detect and localize the open-circuit fault in a four cell flying capacitor inverter, we can certainly say that, the proposed technique is localizing the defective switch very accurately without the need to perform complicated calculations.

6. Bibliographic references

[1] L. Tolbert, F.-Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 36–44, Jan./Feb.1999.

[2] R. H. Baker and L. H. Bannister, "Electric Power Converter,"]U.S. Patent 3 867 643, Feb. 1975.

[3] J. Rodríguez, J. Pontt, G. Alzamora, N. Becker, O. Einenkel, andA. Weinstein, "Novel 20 MW downhill conveyor system using three-levelconverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1093–1100,Oct. 2002.

[4] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for largeelectric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44,Jan./Feb. 1999.

[5] B. Wu, *High-Power Converters and AC Drives*. New York: Wiley-IEEE Press, 2006.

[6] S. Khomfoi and L. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using AI-based techniques," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2954–2968, Dec. 2007.

[7] S. Khomfoi and L. Tolbert, Chapter 31 Multilevel Power Converters (the state of the art of multilevel power converter technology.)

[8] J. Rodríguez, J-S. Lai and F.Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, 2002.

[9] L. Tolbert, F.-Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," IEEE Trans. *Ind. Applic.*, vol. 35, pp. 36–44, Jan./Feb. 1999.

[10] Dixon J., Moran, L., Breton, A., Rios, F., "Multilevel Inverter, Based on Multi-Stage Connection of Three-Level Converters, Scaled in Power of Three", *IEEE Industrial Electronics Conference*, IECON'02, Sevilla, Spain, 5-8 Nov. 2002.

[11] J. Amini and M. Moallem, "A fault-diagnosis and fault-tolerant control scheme for flying capacitor multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1818–1826, 2017.

[12] B. Lu and S.K. Sharma, "A literature review of IGBT fault diagnostic and protection methods for power inverters", *IEEE Trans. on Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, September/October 2009

[13] Cruz, S.M.A.; Ferreira, M.; Mendes, A.M.S.; Cardoso, A.J.M. Analysis and diagnosis ofopen-circuit faults in matrix converters. *IEEE Trans. Ind. Electron.* 2011, *8*, 1648–1661.

[14] Y. Yu, S.-C. Jiang, R.-F. Yang, G. Wang, and D. Xu, "IGBT open circuit fault diagnosis method for inverter," *Proceedings of the CSEE.*, Vol. 31, No. 9, pp. 25-30, Sep. 2011.

[15] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters - an overview," in *IECON 2013*-39th Annual Conference of the IEEE Industrial Electronics Society, 2013, pp. 507–513.

[16] A. E. Ginart, P. W. Kalgren, M. J. Roemer, D. W. Brown, and M. Abbas, "Transistor diagnostic strategies and extended operation under onetransistor trigger suppression in inverter power drives," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 499–506, Feb. 2010.

[17] C. Turpin, P. Baudesson, F. Richardeau, F. Forest, and T. Meynard, "Fault management of multicell converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 988–997, Oct. 2002.

[18] R. Toscano, *Commande et diagnostic des systèmes dynamiques*, Edition Ellipses Paris,2005.

[19] Alavi M., Wang D., Luo M., Short-Circuit Fault Diagnosis for Three-Phase Inverters Based on Voltage-Space Patterns, *IEEE Trans. on Industrial Electronics*, vol. 61, no. 5, pp. 5558-5569 (2014).

[20] R. P. Aguilera, D. E. Quevedo, T. J. Summers, P. Lezana, "Predictive Control Algorithm Robustness for Achieving Fault Tolerance in Multicell Converters," 34th Annual Conference of IEEE Industrial Electronics Society, *in Proc. IEEE IECON 2008*, 10-13 Nov. 2008, pp.3302-3308.

[21] *Fault detection for Modular Multilevel Converters based on Sliding Mode Observer*, Shuai Shao, Patrick W. Wheeler, Member IEEE, Jon C. Clare, Senior Member IEEE, and Alan J. Watson, Member IEEE.

[22] P. Lezana, R. Aguilera, and J. Rodriguez, "Fault detection on multicellconverter based on output voltage frequency analysis," IEEE Trans. Ind.Electron., vol. 56, no. 6, pp. 2275–2283, Jun. 2009

[23] F. Richardeau, Ph. Baudesson, T. Meynard, Failures-Tolerance and Remedial Strategies of a PWM Multicell Inverter, *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 905.912, Nov. 2002.

[24] F. Zidani, D. Diallo, M. Benbouzid, and R. Nait-Said, "A fuzzy-based approach for the diagnosis of fault modes in a voltage-fed PWM inverterinduction motor drive," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp.586–593, Feb. 2008.

[25] M. Trabelsi, M. Boussak, and M. Gossa, "PWM-Switching pattern-based diagnosis scheme for single and multiple open-switch damages in VSI fed induction motor drives," *ISA Trans.*, vol. 51, no. 2, pp. 333–344, Mar. 2012.

[26] S. Karimi, P. Poure, and S. Saadate, "Fast power switch failure detection for fault tolerant voltage source inverters using FPGA," *IET Power Electron.*, vol. 2, no. 4, pp. 346–354, Jul. 2009.

[27] A. Adouni, B. Francoi "Open-circuit fault detection and diagnosis in pulse-width modulation

voltage source inverters based on novel pole voltage approach," *IEEE Trans. Ind. Electronics*. 2015
[28] T. Meynard and H. Foch, "Multi-level conversion : high voltage choppers and voltage source inverters," in , 23rd Annual IEEE Power Electronics Specialists Conference, *1992 PESC '92 Record*, pp. 397–403 vol.1, July 1992.
[29] Shukla, A., Ghosh, A., Joshi, A.: Natural balancing of flying capacitor voltages in multicell inverter under PD carrier-based PWM. *IEEE Trans. Power Electron.* 26(6), 1682–1693 (2011).
[30] J. Amini "An Effortless Space Vector Modulation for N-level Flying Capacitor Multilevel Inverter with Capacitor Voltage Balancing Capability," IEEE Trans. Power Electron., vol. 29, no. 11, pp. 6188-6195, Nov. 2014.
[31] *Multicell Converters: Basic Concepts and Industry Applications*, Thierry A. Meynard, Member IEEE, Henri Foch, Philippe Thomas, Jacques Courault, Roland Jakob, and Manfred Nahrstaedt
[32] Thiziri B. A., "The Control of the Flying Capacitor Multilevel Inverter by PWM," The 3rd International Conference on Power Electronics and their Applications (*ICPEA 2017*), Djelfa, 16-17 Sept. 2017, Algeria.
[33] ADEL CHOUDER "Contribution à la commande des convertisseurs multicellulaires séries," Mémoire de magister 2010 Université de Sétif.
[34] Hanafi Salah ,"Contribution à l'étude et à la commande des structures de conversion d'énergie électrique de type convertisseur multicellulaire,". thèse de doctorat 2016, Université de Sidi Bel-Abbés.
[35] A. Kwasinski and P. T. Krein, *A microgrid-based telecom power system using modular multiple-input dc-dc converters*, Cambridge University Press, 2016.
[36] Braham Ferreira, van der Merwe, Wim, *The Principles of Electronic and Electromechanic Power Conversion: A Systems Approach*, Wiley-IEEE.
[37] F. Huang, F. Flett, "IGBT fault protection based on di/dt feedback control," in Proc. *IEEE Power Electron. Spec. Conf.*, pp. 1478-1484, 2007.

Funding Sources

This work was supported by the Applied Automation and Industrial Diagnostics Laboratory (LAADI), Ziane Achour, University of Djelfa, in Algeria, and financially co-sponsored by The General Directorate of Scientific Research and Technological Development (DGRSDT), Algeria under the Doctoral Habilitation approved by the decision of the Ministry of High Education and Scientific Research (MESRS) decision number 333 of 12th July 2015.

Authors' Biographies

Miss **BEN ALI Thiziri** was born in Hassi Bahbah, Djelfa, Algeria, in 1992.
She received her Licence degree in automatic control from the University of M'hamed Bouguara Boumerdes, Algeria, in 2013 and the Master degree in the same option from the University of Boumerdes, Algeria, in 2015.
She is working toward the PhD degree at University Ziane Achour of Djelfa, Algeria: Applied Automation and Industrial Diagnostic Laboratory,
Her main fields of interest are power electronic, industrial diagnostics, fault detection in power converters.
e-mail address: thizirihala@gmail.com

Prof. **KOUZOU Abdellah** (IEEE Senior member & IACSIT Senior member, IFAC, IAENG & IISRO member, IEEE-HKN Alumni Member) was born in Djelfa, Algeria in 1964.
He is a collaborator researcher at Texas A&M University at Qatar.
He has participated in several research projects and has led several research projects. He is the founder of the Power Electronics and Power Quality research group at the Applied Automation and Industrial Diagnostic Laboratory, University of Djelfa in Algeria. He is the supervisor of many PhD Students in Algeria. He is member of the Smart Grid Centre at Qatar SGC-Q.
He is a member of many editorial boards for several scientific journals and a member of the scientific and steering committees in several national and international conferences. He is the coordinator of the Algerian IEEE Power Electronics Chapter and the chair of the sub-committee on FACTs and HVDC under the international committee PETC/IEEE-IES. He was a plenary and an invited keynote speaker and session chair in several national and international conferences and an expert in several national and international scientific activities and project evaluations.
He has published more than 250 papers.
His main research interests include Active Power Filtering techniques, Power Quality issues, Power Electronics Devices, Application of Power electronics in Renewable Energies, Smart Grid, reliability and diagnostics in power electronics converters.
e-mail address: kouzouabdellah@ieee.org

Prof. **HAFAIFA Ahmed** was born in Algeria in 1974.
He received the State Engineer degree in 2000 on Applied Automation, the Magister degree in 2004 on Applied Automation and control systems and the PhD on Applied Automation and Signal Processing in 2010 from the UMBB Boumerdes University.
He is Full Professor at the Science and Technology Faculty of the University of Djelfa, Algeria. He has participated in several international research projects and has led several national research projects. Currently he is the Director of the Applied Automation and Industrial Diagnostic Laboratory of the University of Djelfa. He is the coordinator of several industrial research projects within the applied automatic and reliability of industrial systems. His research area of interests includes the modelling and control in industrial systems, the diagnosis and new reliability engineering, fault detection and isolation in industrials process, intelligent system based on fuzzy logic and neural networks.
He is acting as an expert in several national and internationals commissions and collaboration research activities. He has published many national/international conferences and journals papers.
e-mail address: hafaifa@hotmail.com

Mr **Ali TETA**, was born in Djelfa, Algeria in 1991.
He received the License degree in electrical machine and the Master degree in power electronics and quality of electrical energy from the University of Djelfa in 2014 and 2016 respectively.
Now he is a member in the Applied Automation and Industrial Diagnostics Laboratory (LAADI), University of Djelfa 17000 DZ, Algeria, where he is preparing his Ph.D. doctorate degrees in power electronics and quality of electrical energy. His main fields of interest is the compensation of the harmonics and the improvement of power factor.
e-mail address: a.teta@univ-djelfa.dz